AAT4672

SmartSwitch™

Power Supply Selector Switch

General Description

The AAT4672 SmartSwitch™ is a member of AnalogicTech's Application Specific Power Management IC™ family. This device is a dual input, single output power supply selector switch, designed to operate from USB ports, AC adapter inputs, batteries, or any other power supply with an input voltage up to 6V.

The AAT4672 connects the supply on the MAIN pin to the OUT pin through a very low on-resistance power MOSFET when the device is enabled, the MAIN pin voltage is higher than the under voltage lockout (UVLO) threshold, and MAIN pin voltage is greater than the AUX pin voltage plus 200mV. The AUX pin connects to the OUT pin only when the MAIN pin voltage drops 0.2V below the AUX pin voltage and the AUX pin voltage is greater than the UVLO threshold. If both input supplies (MAIN/AUX) are below the UVLO threshold, then the OUT pin floats.

The two internal power switches are current limited and the thresholds can be programmed through resistors on the IMAIN and IAUX pins respectively. A power level selection pin, PWRSEL, is provided to toggle the AUX current limit between 100% and 20% of the current limit setting programmed by the resistor on the IAUX pin. This is particularly useful for USB applications where the power supply can be powered by either a 500mA or a 100mA USB port.

The AAT4672 is available in a thermally enhanced, space-saving, Pb-free 12-pin TSOPJW package and is specified for operation over the -40°C to +85°C temperature range.

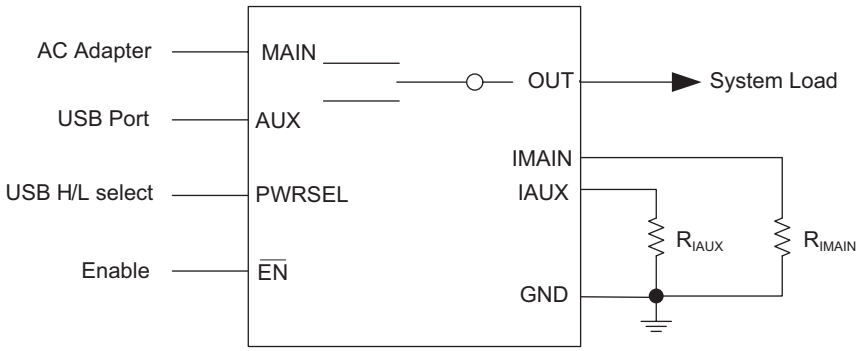
Features

- Input Voltage Supply Range: 2.5V to 6V
- High Level of Integration:
  - Reverse Blocking Diode
  - Current Sensing
  - Programmable Current Limiting
  - Automatic Power Supply Switching
- Break-Before-Make Switch-Over
  - Minimum Output Voltage Drop During Change-Over
- Shutdown Current < 1µA
- Thermal Protection
- TSOPJW-12 Package

Applications

- Bluetooth™ Headsets
- Cell Phones
- Digital Still Cameras
- MP3 Players
- Personal Data Assistants (PDAs)

Typical Application

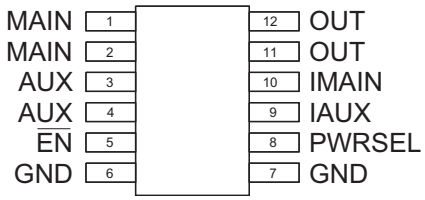


Pin Descriptions

Pin Number	Name	Type	Function
1, 2	MAIN	I	Power supply 1 input.
3, 4	AUX	I	Power supply 2 input.
5	$\overline{EN}$	I	Enable pin, active low.
6, 7	GND	I/O	Ground.
8	PWRSEL	I	Power level select input for AUX-OUT switch. Logic "0": 20% of the current limit programmed by R_{IAUX} Logic "1": 100% of the current limit programmed by R_{IAUX}
9	IAUX	I	AUX-OUT switch current limit set input.
10	IMAIN	I	MAIN-OUT switch current limit set input.
11, 12	OUT	O	Output pin.

Pin Configuration

TSOPJW-12
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_N	[MAIN, AUX] to GND	-0.3 to 6.5	V
V_X	[OUT, $\overline{EN}$, IMAIN, IAUX, PWRSEL] to GND	-0.3 to V_N + 0.3	V
T_{LEAD}	Maximum Soldering Temperature (at Leads)	300	°C
I_{OUT}	Maximum Output Current	3	A

Thermal Information[2]

Symbol	Description	Value	Units
θ_{JA}	Maximum Thermal Resistance	160	°C/W
P_D	Maximum Power Dissipation	625	mW
T_J	Operating Junction Temperature Range	-40 to 150	°C

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on a FR4 board.

Electrical Characteristics[1]

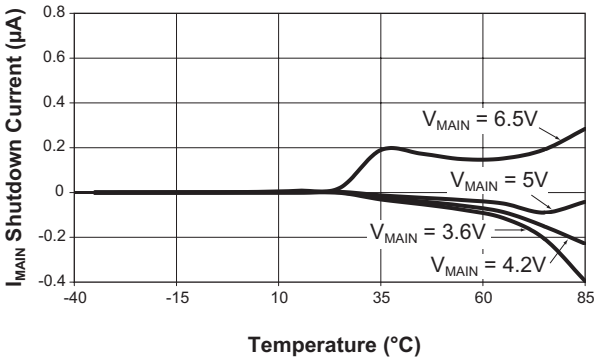
$V_{MAIN/AUX}$ = 5V, T_A = -40 to +85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions		Min	Typ	Max	Units
Operation							
V_{MAIN}	MAIN Operating Voltage Range			2.5		6	V
V_{AUX}	AUX Operating Voltage Range			2.5		6	V
$V_{MAIN-AUX}$	MAIN Switch-Over Threshold (Input Voltage Difference)	MAIN, AUX > 2.5V		V_{AUX} + 0.15	V_{AUX} + 0.2	V_{AUX} +0.25	V
V_{UVLO_MAIN}	MAIN Under-Voltage Lockout	Rising edge				2.3	V
		Hysteresis			0.1		
V_{UVLO_AUX}	AUX Under-Voltage Lockout	Rising edge				2.3	V
		Hysteresis			0.1		
I_{MAIN_OP}	MAIN Normal Operating Current	V_{MAIN} = 5V, $V_{\overline{EN}}$ = 0V			10	30	µA
I_{MAIN_SHDN}	MAIN Shutdown Mode Current	V_{MAIN} = $V_{\overline{EN}}$ = 5V, OUT open				1	µA
I_{MAIN_SLP}	MAIN Sleep Current	V_{MAIN} = 2.5V, V_{AUX} = 5V, $V_{\overline{EN}}$ = 0V			1	5	µA
I_{AUX_OP}	AUX Normal Operating Current	V_{AUX} = 5V, $V_{\overline{EN}}$ = 0V			10	30	µA
I_{AUX_SHDN}	AUX Shutdown Mode Current	V_{AUX} = $V_{\overline{EN}}$ = 5V, OUT open				1	µA
I_{AUX_SLP}	AUX Sleep Current	V_{MAIN} = 5V, V_{AUX} = 2.5V, $V_{\overline{EN}}$ = 0V			1	5	µA
Power Switches							
$R_{DS(ON)\ MAIN}$	MAIN-to-OUT FET On-Resistance	V_{MAIN} = 5.0V			0.12		Ω
		V_{MAIN} = 3.5V			0.14		
$R_{DS(ON)\ AUX}$	AUX-to-OUT FET On-Resistance	V_{AUX} = 5.0V			0.12		Ω
		V_{AUX} = 3.5V			0.14		
V_{DROOP_OUT}	OUT Voltage Droop from the Lower Voltage of MAIN and AUX, When Switching Over Between MAIN and AUX	$I_{O(OUT)}$ = 0.5A, $C_{O(OUT)}$ = 10µF			150		mV
Current Regulation							
t_{SOFT_START}	Soft-Start Delay	Delay of start from $\overline{EN}$, or UVLO			100		µs
$I_{LIM\_MAIN\_range}$	MAIN Current Limit Range			0.2		2.0	A
$I_{LIM\_AUX\_range}$	AUX Current Limit Range	PWRSEL = 5V		0.2		2.0	A
		PWRSEL = 0V		0.04		0.4	
I_{LIM_MAIN}	MAIN Current Limit Accuracy	R_{IAUX} = 100kΩ		0.8	1	1.2	A
I_{LIM_AUX}	AUX Current Limit Accuracy	R_{IMAIN} = 100kΩ	PWRSEL = 5V	0.8	1	1.2	A
			PWRSEL = 0V	0.18	0.2	0.22	
Logic Control / Protection							
$V_{IH(\overline{EN})}$	Logic High Threshold			1.6			V
$V_{IL(\overline{EN})}$	Logic Low Threshold					0.4	V
T_{SHDN}	Chip Thermal Shutdown Temperature	Threshold			140		°C
		Hysteresis			15		

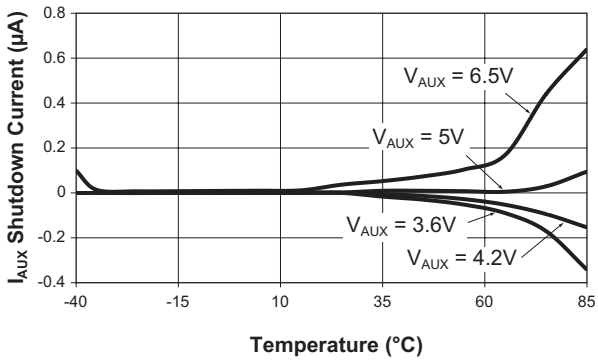
1. The output charge voltage accuracy is specified over the 0° to 70°C ambient temperature range; operation over the -25°C to +85°C temperature range is guaranteed by design.

Typical Characteristics

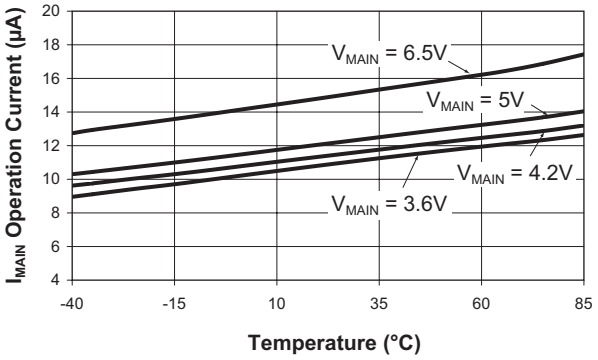
I_{MAIN} Shutdown Current vs. Temperature



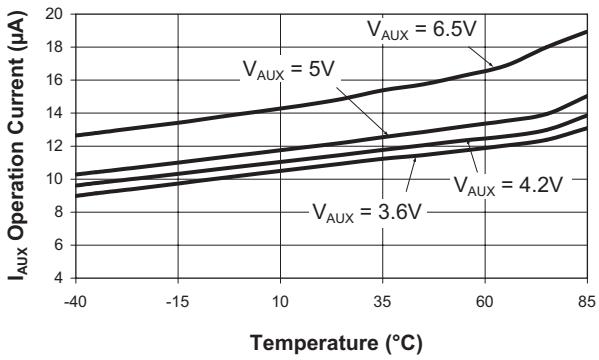
I_{AUX} Shutdown Current vs. Temperature



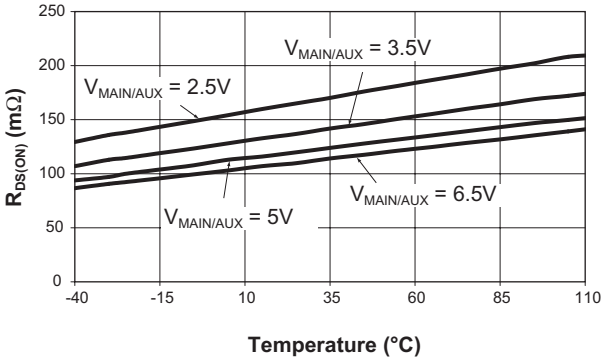
I_{MAIN} Operation Current vs. Temperature
(I_{OUT} = 0A)



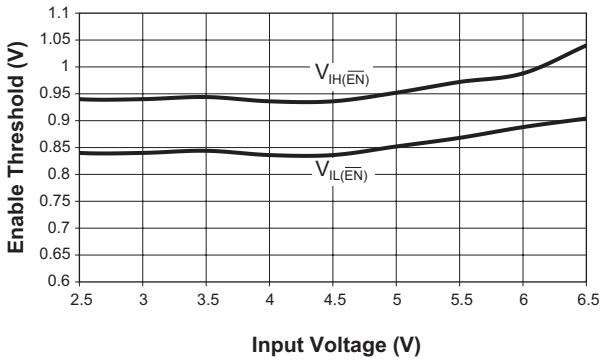
I_{AUX} Operation Current vs. Temperature
(I_{OUT} = 0A)



$R_{DS(ON)}$ vs. Temperature

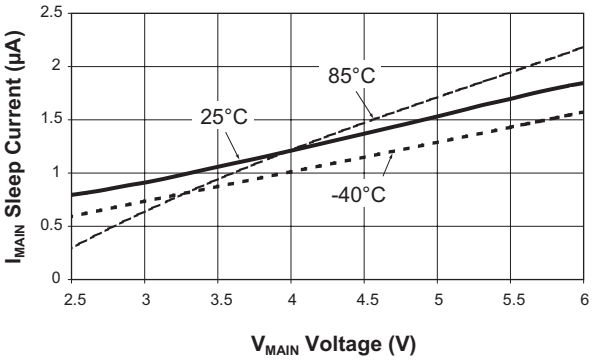


Enable Threshold vs. Input Voltage

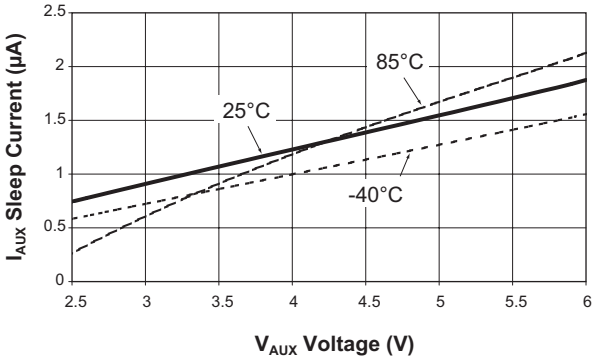


Typical Characteristics

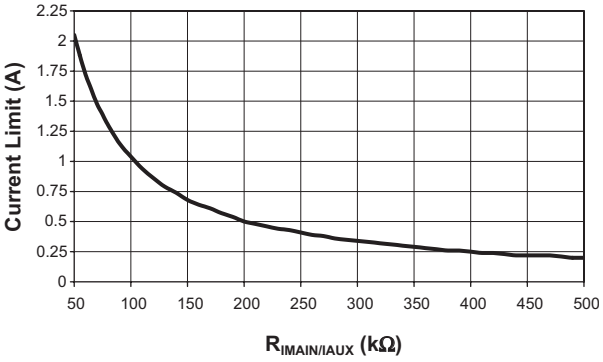
I_{MAIN} Sleep Current vs. V_{MAIN} Voltage
(V_{AUX} = 6.5V)



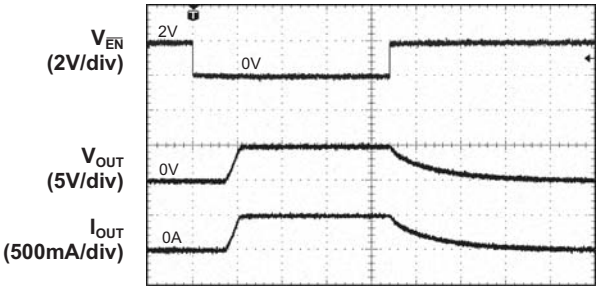
I_{AUX} Sleep Current vs. V_{AUX} Voltage
(V_{MAIN} = 6.5V)



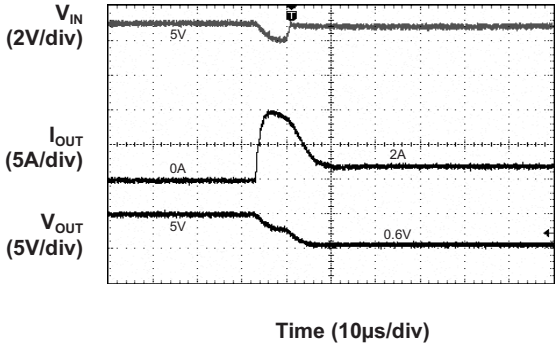
Current Limit vs. $R_{IMAIN/IAUX}$
(V_{MAIN} = 5V; V_{AUX} = 3.3V; V_{OUT} = V_{MAIN} or V_{OUT} = V_{AUX})



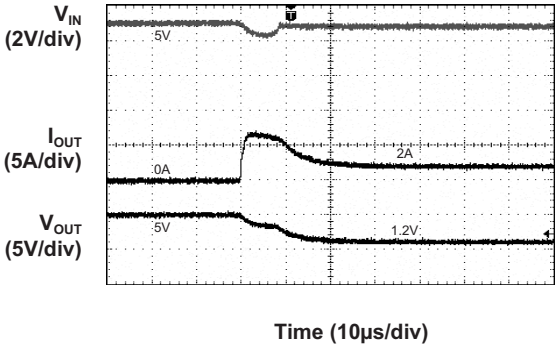
Turn-On/Off Response
(R_{OUT} = 10Ω; V_{MAIN} = 5V)



Short Circuit Through 0.3Ω Response

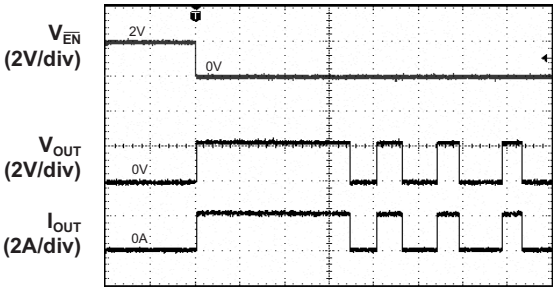


Short Circuit Through 0.6Ω Response



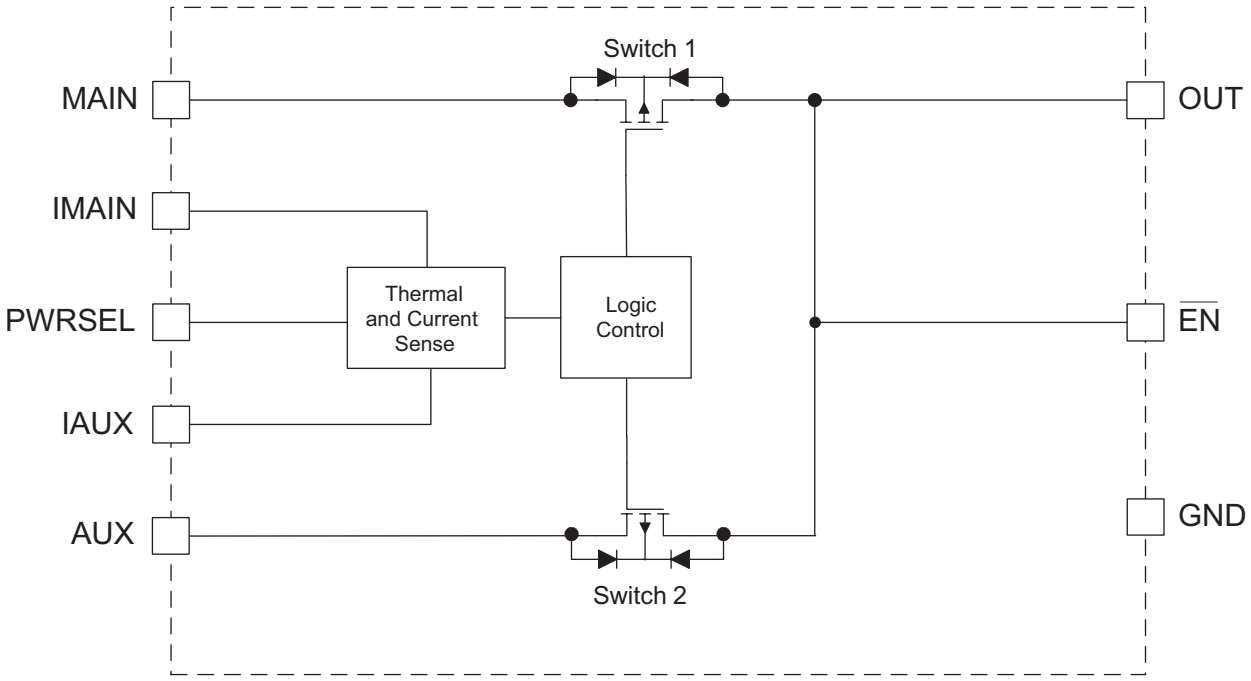
Typical Characteristics

Thermal Shutdown Response
(V_{MAIN} = 5V)



Time (40ms/div)

Functional Block Diagram



Truth Table

Y = Yes, N = No, X = don't care.

Input Conditions			AAT4672
V_{MAIN} > UVLO	V_{AUX} > UVLO	V_{MAIN} > V_{AUX} + 0.2V	V_{OUT}
N	N	X	Floating
Y	N	X	V_{MAIN}
N	Y	X	V_{AUX}
Y	Y	Y	V_{MAIN}
Y	Y	N	V_{AUX}

Functional Description

To power the OUT pin, at least one of the two input supplies (MAIN/AUX) must be greater than the UVLO threshold. If only one supply is greater than the UVLO threshold, the load will be connected to that particular supply when the device is enabled. If both supplies are above the UVLO threshold, the AAT4672 will connect the supply from the MAIN pin to the OUT pin when the device is enabled and the MAIN voltage is greater than the AUX voltage plus 0.2V (typical); otherwise, the AAT4672 will connect the supply from the AUX pin to the OUT pin.

The two internal power switches are current limited; the current limits are programmed by the resistors on the IMAIN and IAUX pins respectively.

Applications Information

Input Capacitors

A 1µF or greater capacitor is generally recommended between MAIN and GND (C_{MAIN}), and between AUX and GND (C_{AUX}). An input capacitor is not required for basic operation; however, it is useful in preventing load transients from affecting up-stream circuits. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{MAIN}/C_{AUX}. There is no specific capacitor equivalent series resistance (ESR) requirement for C_{MAIN}/C_{AUX}. However, for higher current operation, ceramic capacitors are recommended for C_{MAIN}/C_{AUX} due to their inherent capability over tantalum capacitors to withstand

input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

A 1µF or greater capacitor is required between OUT and GND (C_{OUT}). As with the input capacitor, there is no specific capacitor ESR requirement. If desired, C_{OUT} may be increased to accommodate any load transient condition.

EN Input

The AAT4672 is enabled when $V_{\overline{EN}}$ is ≤ 0.4V (logic '0'); conversely, the AAT4672 is disabled when $V_{\overline{EN}}$ is ≥ 1.6V (logic '1').

PWRSEL Input

When V_{PWRSEL} is ≤ 0.4V (logic '0') the AUX-OUT current limit is 20% of the current limit value programmed by R_{IAUX}; when V_{PWRSEL} is ≥ 1.6V (logic '1'), the AUX-OUT current limit is 100% of the current limit value programmed by R_{IAUX}.

Current Limit Resistor Selection

The current limits for power supply 1 and power supply 2 inputs are set by resistors between I_{MAIN}/I_{AUX} and GND. The following equation can be used to select the appropriate resistor for a particular current limit:

$$I_{CLMAIN/AUX} = \left(\frac{V_{IMAIN/IAUX}}{R_{IMAIN/IAUX}}\right) \cdot 200k$$

$I_{CLIMAIN/AUX}$	Current limit for MAIN and/or AUX pins respectively
$V_{IMAIN/IAUX}$	Internally Regulated Voltage [0.5V ± 20%] on the IMAIN and IAUX pins respectively
$R_{IMAIN/IAUX}$	IMAIN and/or IAUX Resistor
200k	Internal Gain Factor

Design Example

A particular application requires that the current limit for MAIN be set to 2A and the current limit for AUX be set to 0.2A. What value of resistor is required for the IMAIN and IAUX pins respectively?

For MAIN (power supply 1 input):

$$R_{IMAIN} = \left(\frac{V_{IMAIN}}{I_{CLMAIN}}\right) \cdot 200k$$

$$= \left(\frac{0.5V}{2A}\right) \cdot 200k$$

$$= 50k\Omega \text{ (49.9k}\Omega \text{ standard value)}$$

For AUX (power supply 2 input):

$$R_{IAUX} = \left(\frac{V_{IAUX}}{I_{CLAUX}}\right) \cdot 200k$$

$$= \left(\frac{0.5V}{0.2A}\right) \cdot 200k$$

$$= 500k\Omega \text{ (499.9k}\Omega \text{ standard value)}$$

Thermal Considerations

Since the AAT4672 has an internal current limit and over-temperature protection(thermal shutdown), junction temperature is rarely a concern. However, if the application requires large currents in a high temperature environment, it is possible that temperature rather than current limit will be the dominant regulating condition. In these applications, the maximum current available without risk of an over-temperature condition must be calculated. The maximum internal temperature while current limit is not active can be calculated using Equation 1 (Eq. 1).

Eq. 1: $T_{J(MAX)} = I_{MAX}2 \cdot R_{DS(ON)(MAX)} \cdot R_{\theta JA} + T_{A(MAX)}$

In Equation 1, I_{MAX} is the maximum current required by the load. $R_{DS(ON)(MAX)}$ is the maximum rated $R_{DS(ON)}$ of the AAT4672 at high temperatures (consult the "R_{DSON} vs. Temperature" performance graph in the "Typical Characteristics" section of this datasheet). For estimating the $R_{DS(ON)(MAX)}$ use the data on the "R_{DSON} vs Temperature" performance graph and increase the value from the performance graph by 50%. $R_{\theta JA}$ is the thermal resistance between the AAT4672 die and the printed circuit board (PCB) onto which it is mounted; $R_{\theta JA}$ is the thermal resistance of the TSOPJW-12 package. $T_{A(MAX)}$ is the maximum ambient temperature that the PCB under the AAT4672 would be if the AAT4672 were not dissipating power. Equation 1 can be rearranged to solve for I_{MAX}, into Equation 2 (Eq. 2).

$$\textbf{Eq. 2: } I_{MAX} = \sqrt{\frac{T_{SD(MIN)} - T_{A(MAX)}}{R_{DS(ON)(MAX)} \cdot R_{\Theta JA}}}$$

$T_{SD(MIN)}$ is the minimum temperature required to activate the AAT4672 over-temperature protection (thermal shutdown). With typical specification of 140°C, 125°C is a safe minimum value to use.

For example, for a 2.5V input power supply application that is specified to operate in 50°C environments where the PCB operates at temperatures as high as 85°C. The application is sealed and its PCB is small, causing $R_{\theta JA}$ to be approximately 160°C/W. The $R_{DS(ON)(MAX)}$ is estimated to be 300mΩ (from the "$R_{DS(ON)}$ vs. Temperature" performance graph, where V_{IN} = 2.5V at 85°C plus 50%). To find the maximum current (I_{MAX}) for this application, use Equation 2:

$$I_{MAX} = \sqrt{\frac{125°C - 85°C}{300m\Omega \cdot 160°C/W}} = 0.913A$$

PCB Layout Recommendations

For proper thermal management, to minimize PCB trace resistance, and to take advantage of the low $R_{DS(ON)}$ values of the two internal power switches in the AAT4672, certain circuit board layout rules should be followed: MAIN, AUX, and OUT should be routed using wider than normal traces. The two MAIN pins (1 and 2) and two AUX pins (3 and 4) should be connected to the same wide PCB trace; and GND should be connected to a ground plane. For best performance, input capacitors (C_{MAIN}, C_{AUX}) and output capacitor (C_{OUT}) should be placed as close to the package pins as possible. The AAT4672 evaluation board layout follows the printed circuit board layout recommendations and can be used as an example of an optimal board layout.

Evaluation Board Schematic

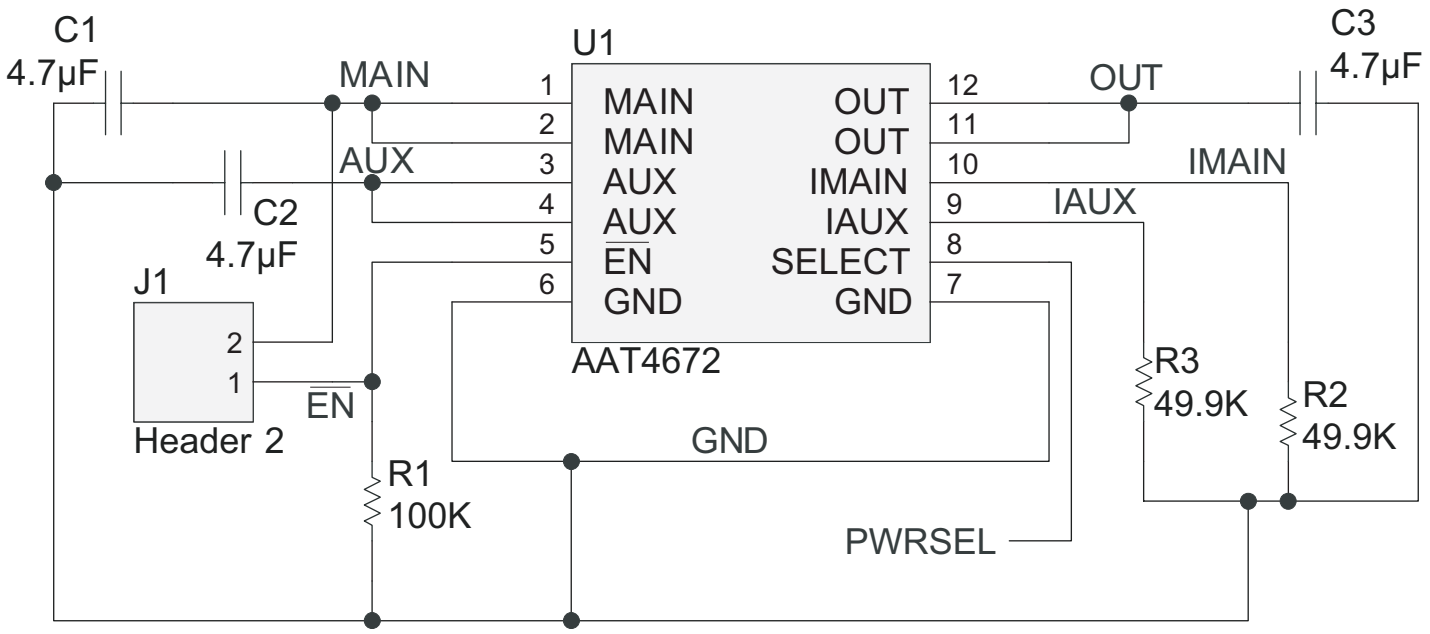


Figure 1: AAT4672 Evaluation Board Schematic.

Evaluation Board Layout

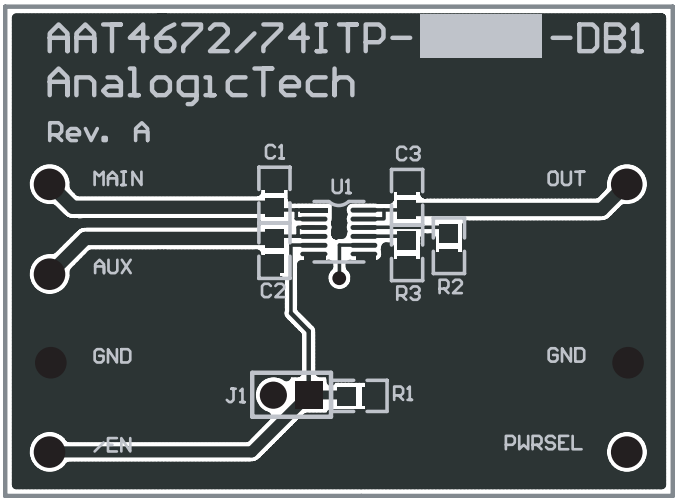


Figure 2: AAT4672 Evaluation Board Top Side Layout.

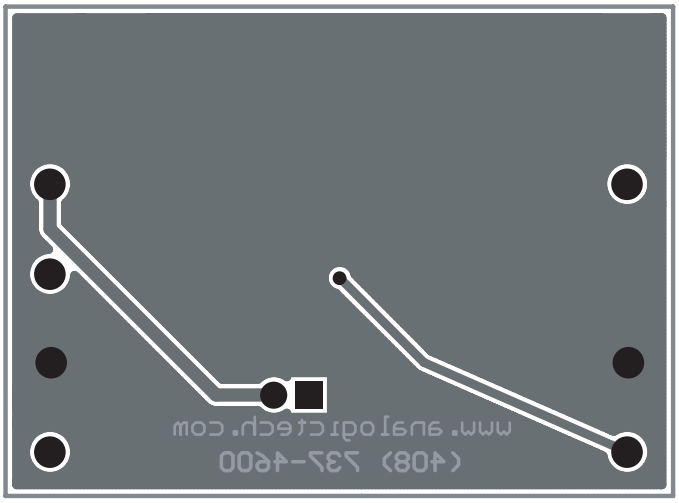


Figure 3: AAT4672 Evaluation Board Bottom Side Layout.

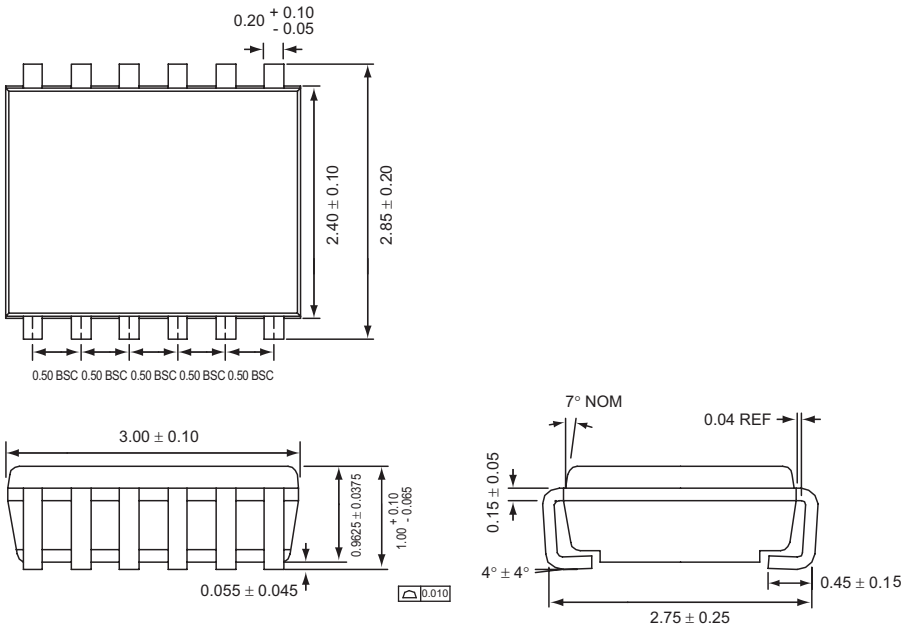
Ordering Information

Package	Marking[1]	Part Number (Tape and Reel)[2]
TSOPJW-12	ZWXYY	**AAT4672ITP-T1**

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/about/quality.aspx.

Package Information

TSOPJW-12



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

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3230 Scott Boulevard, Santa Clara, CA 95054
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Fax (408) 737-4611

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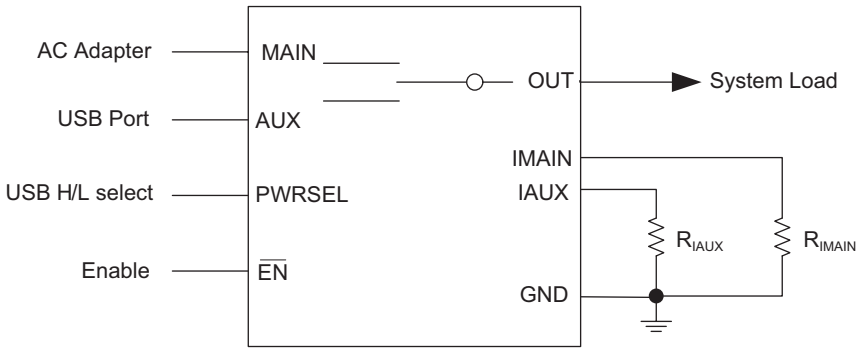

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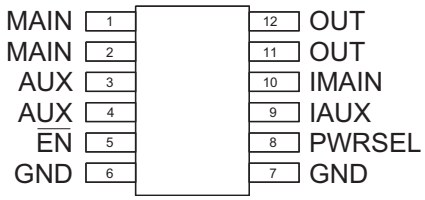
10	IMAIN	I	MAIN-OUT switch current limit set input.
11, 12	OUT	O	Output pin.

Pin Configuration

TSOPJW-12
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_N	[MAIN, AUX] to GND	-0.3 to 6.5	V
V_X	[OUT, $\overline{EN}$, IMAIN, IAUX, PWRSEL] to GND	-0.3 to V_N + 0.3	V
T_{LEAD}	Maximum Soldering Temperature (at Leads)	300	°C
I_{OUT}	Maximum Output Current	3	A

Thermal Information[2]

Symbol	Description	Value	Units
θ_{JA}	Maximum Thermal Resistance	160	°C/W
P_D	Maximum Power Dissipation	625	mW
T_J	Operating Junction Temperature Range	-40 to 150	°C

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on a FR4 board.

Electrical Characteristics[1]

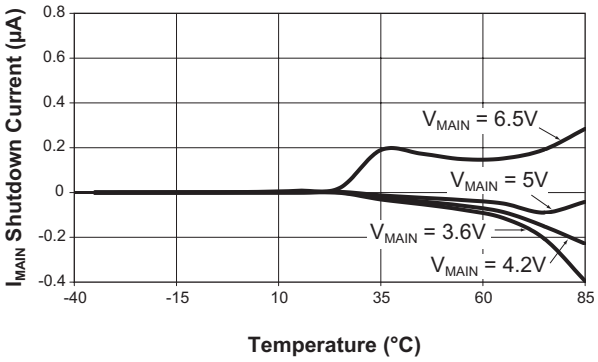
$V_{MAIN/AUX}$ = 5V, T_A = -40 to +85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions		Min	Typ	Max	Units
Operation							
V_{MAIN}	MAIN Operating Voltage Range			2.5		6	V
V_{AUX}	AUX Operating Voltage Range			2.5		6	V
$V_{MAIN-AUX}$	MAIN Switch-Over Threshold (Input Voltage Difference)	MAIN, AUX > 2.5V		V_{AUX} + 0.15	V_{AUX} + 0.2	V_{AUX} +0.25	V
V_{UVLO_MAIN}	MAIN Under-Voltage Lockout	Rising edge				2.3	V
		Hysteresis			0.1		
V_{UVLO_AUX}	AUX Under-Voltage Lockout	Rising edge				2.3	V
		Hysteresis			0.1		
I_{MAIN_OP}	MAIN Normal Operating Current	V_{MAIN} = 5V, $V_{\overline{EN}}$ = 0V			10	30	µA
I_{MAIN_SHDN}	MAIN Shutdown Mode Current	V_{MAIN} = $V_{\overline{EN}}$ = 5V, OUT open				1	µA
I_{MAIN_SLP}	MAIN Sleep Current	V_{MAIN} = 2.5V, V_{AUX} = 5V, $V_{\overline{EN}}$ = 0V			1	5	µA
I_{AUX_OP}	AUX Normal Operating Current	V_{AUX} = 5V, $V_{\overline{EN}}$ = 0V			10	30	µA
I_{AUX_SHDN}	AUX Shutdown Mode Current	V_{AUX} = $V_{\overline{EN}}$ = 5V, OUT open				1	µA
I_{AUX_SLP}	AUX Sleep Current	V_{MAIN} = 5V, V_{AUX} = 2.5V, $V_{\overline{EN}}$ = 0V			1	5	µA
Power Switches							
$R_{DS(ON)\ MAIN}$	MAIN-to-OUT FET On-Resistance	V_{MAIN} = 5.0V			0.12		Ω
		V_{MAIN} = 3.5V			0.14		
$R_{DS(ON)\ AUX}$	AUX-to-OUT FET On-Resistance	V_{AUX} = 5.0V			0.12		Ω
		V_{AUX} = 3.5V			0.14		
V_{DROOP_OUT}	OUT Voltage Droop from the Lower Voltage of MAIN and AUX, When Switching Over Between MAIN and AUX	$I_{O(OUT)}$ = 0.5A, $C_{O(OUT)}$ = 10µF			150		mV
Current Regulation							
t_{SOFT_START}	Soft-Start Delay	Delay of start from $\overline{EN}$, or UVLO			100		µs
$I_{LIM\_MAIN\_range}$	MAIN Current Limit Range			0.2		2.0	A
$I_{LIM\_AUX\_range}$	AUX Current Limit Range	PWRSEL = 5V		0.2		2.0	A
		PWRSEL = 0V		0.04		0.4	
I_{LIM_MAIN}	MAIN Current Limit Accuracy	R_{IAUX} = 100kΩ		0.8	1	1.2	A
I_{LIM_AUX}	AUX Current Limit Accuracy	R_{IMAIN} = 100kΩ	PWRSEL = 5V	0.8	1	1.2	A
			PWRSEL = 0V	0.18	0.2	0.22	
Logic Control / Protection							
$V_{IH(\overline{EN})}$	Logic High Threshold			1.6			V
$V_{IL(\overline{EN})}$	Logic Low Threshold					0.4	V
T_{SHDN}	Chip Thermal Shutdown Temperature	Threshold			140		°C
		Hysteresis			15		

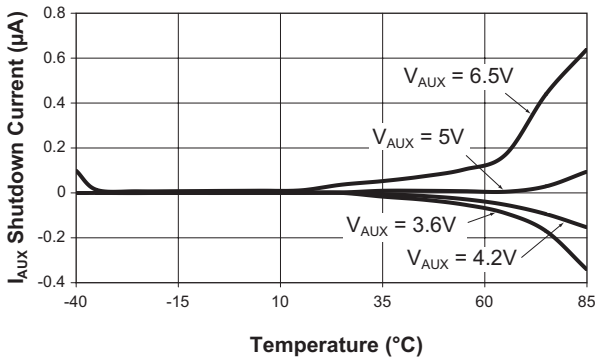
1. The output charge voltage accuracy is specified over the 0° to 70°C ambient temperature range; operation over the -25°C to +85°C temperature range is guaranteed by design.

Typical Characteristics

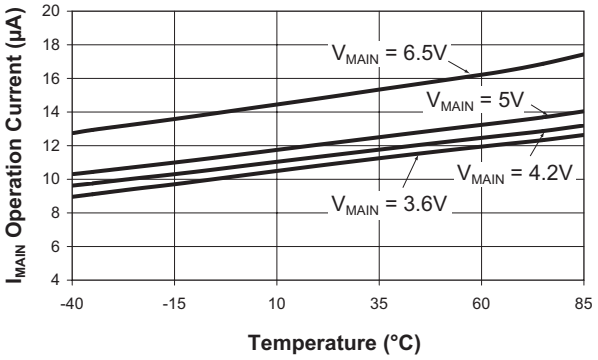
I_{MAIN} Shutdown Current vs. Temperature



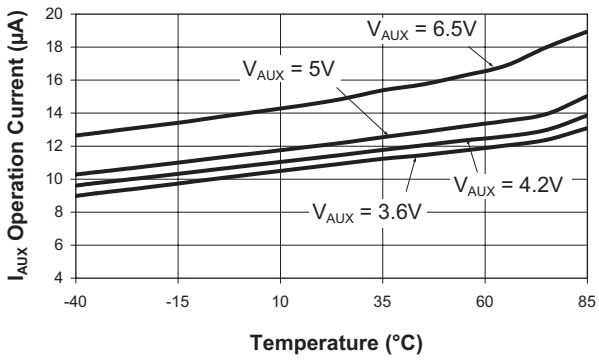
I_{AUX} Shutdown Current vs. Temperature



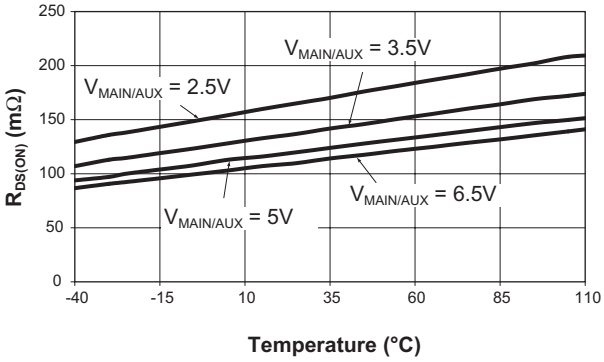
I_{MAIN} Operation Current vs. Temperature
(I_{OUT} = 0A)



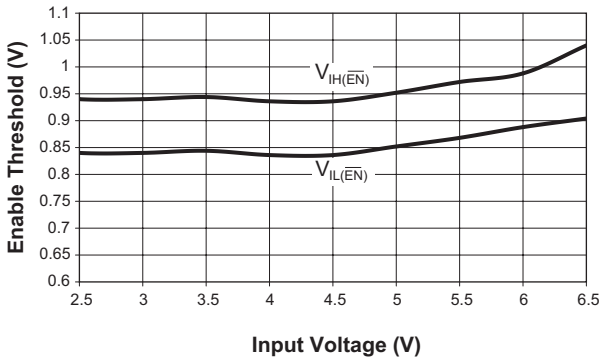
I_{AUX} Operation Current vs. Temperature
(I_{OUT} = 0A)



$R_{DS(ON)}$ vs. Temperature

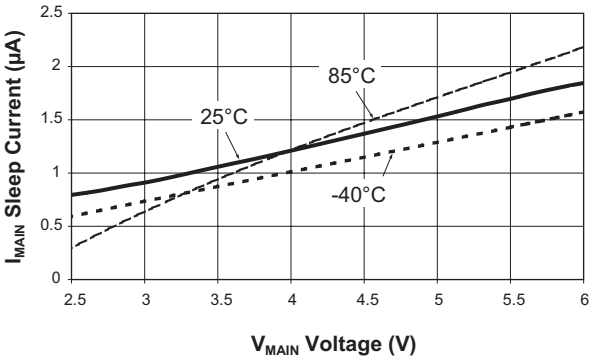


Enable Threshold vs. Input Voltage

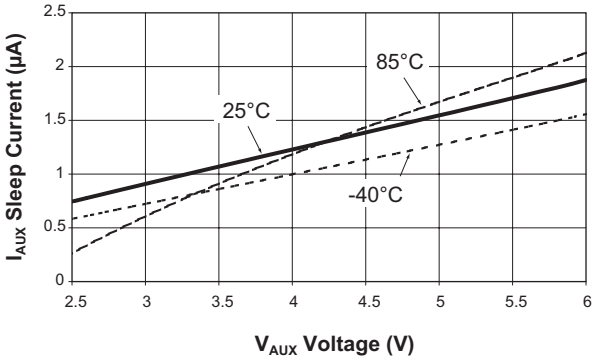


Typical Characteristics

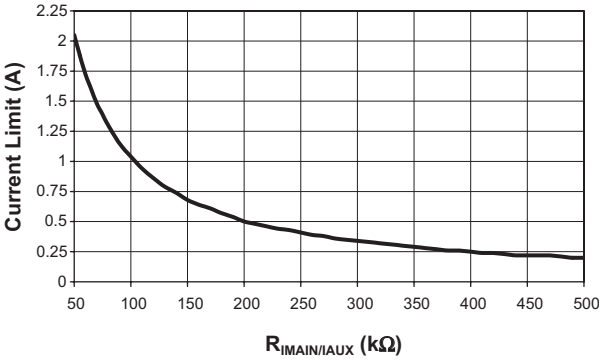
I_{MAIN} Sleep Current vs. V_{MAIN} Voltage
(V_{AUX} = 6.5V)



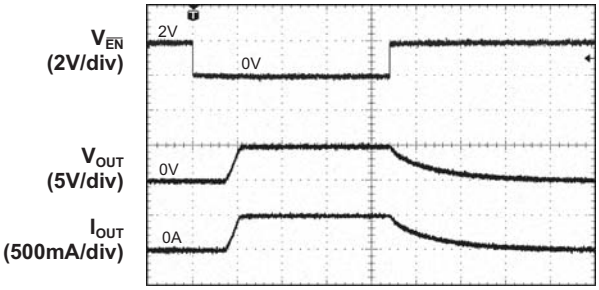
I_{AUX} Sleep Current vs. V_{AUX} Voltage
(V_{MAIN} = 6.5V)



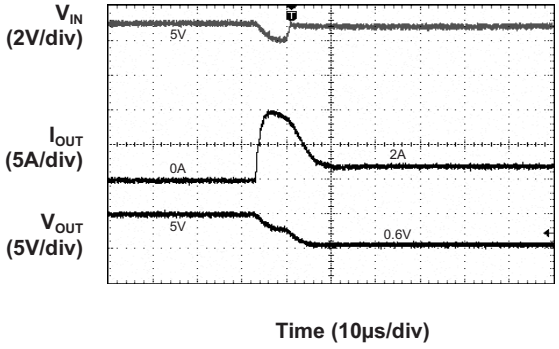
Current Limit vs. $R_{IMAIN/IAUX}$
(V_{MAIN} = 5V; V_{AUX} = 3.3V; V_{OUT} = V_{MAIN} or V_{OUT} = V_{AUX})



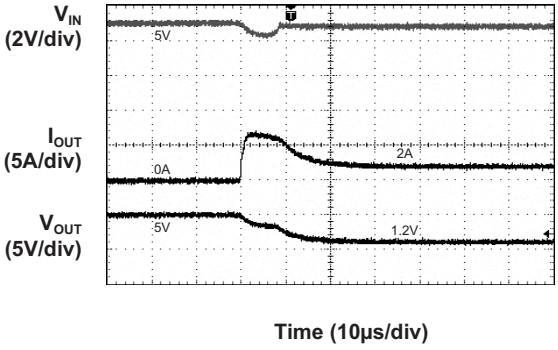
Turn-On/Off Response
(R_{OUT} = 10Ω; V_{MAIN} = 5V)



Short Circuit Through 0.3Ω Response

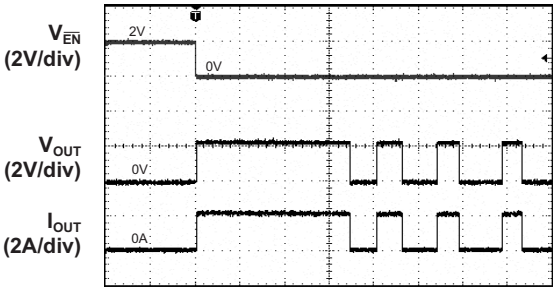


Short Circuit Through 0.6Ω Response



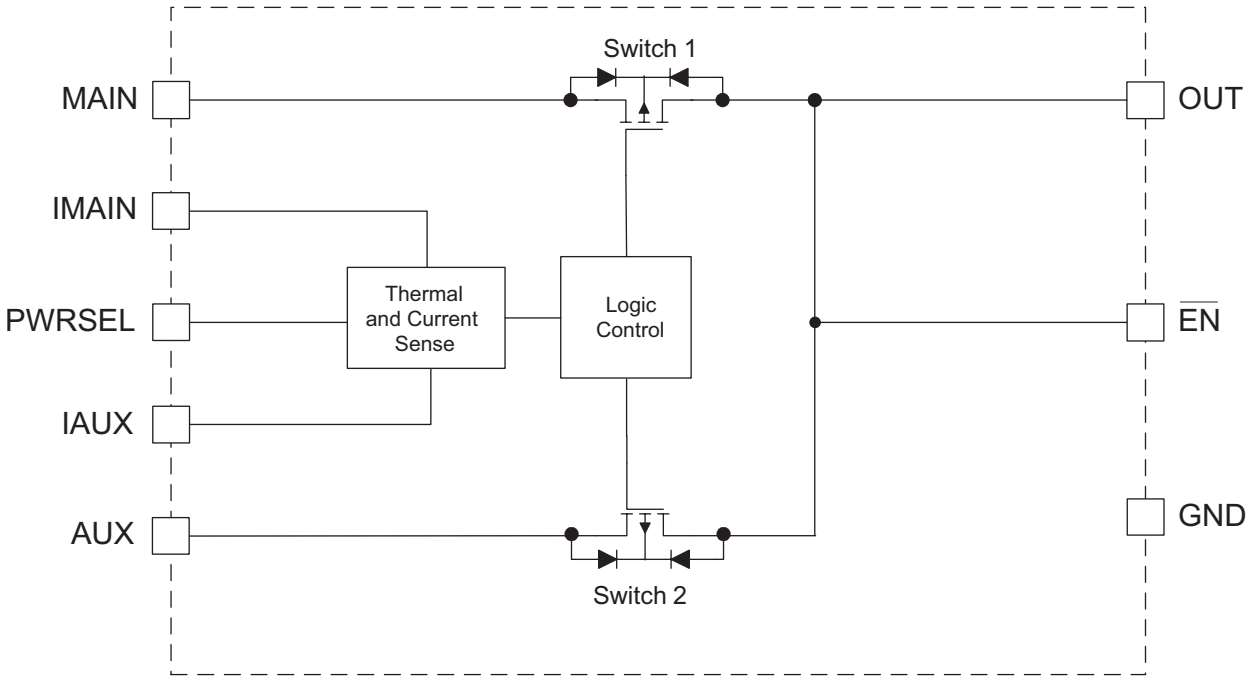
Typical Characteristics

Thermal Shutdown Response
(V_{MAIN} = 5V)



Time (40ms/div)

Functional Block Diagram



Truth Table

Y = Yes, N = No, X = don't care.

Input Conditions			AAT4672
V_{MAIN} > UVLO	V_{AUX} > UVLO	V_{MAIN} > V_{AUX} + 0.2V	V_{OUT}
N	N	X	Floating
Y	N	X	V_{MAIN}
N	Y	X	V_{AUX}
Y	Y	Y	V_{MAIN}
Y	Y	N	V_{AUX}

Functional Description

To power the OUT pin, at least one of the two input supplies (MAIN/AUX) must be greater than the UVLO threshold. If only one supply is greater than the UVLO threshold, the load will be connected to that particular supply when the device is enabled. If both supplies are above the UVLO threshold, the AAT4672 will connect the supply from the MAIN pin to the OUT pin when the device is enabled and the MAIN voltage is greater than the AUX voltage plus 0.2V (typical); otherwise, the AAT4672 will connect the supply from the AUX pin to the OUT pin.

The two internal power switches are current limited; the current limits are programmed by the resistors on the IMAIN and IAUX pins respectively.

Applications Information

Input Capacitors

A 1µF or greater capacitor is generally recommended between MAIN and GND (C_{MAIN}), and between AUX and GND (C_{AUX}). An input capacitor is not required for basic operation; however, it is useful in preventing load transients from affecting up-stream circuits. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{MAIN}/C_{AUX}. There is no specific capacitor equivalent series resistance (ESR) requirement for C_{MAIN}/C_{AUX}. However, for higher current operation, ceramic capacitors are recommended for C_{MAIN}/C_{AUX} due to their inherent capability over tantalum capacitors to withstand

input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

A 1µF or greater capacitor is required between OUT and GND (C_{OUT}). As with the input capacitor, there is no specific capacitor ESR requirement. If desired, C_{OUT} may be increased to accommodate any load transient condition.

EN Input

The AAT4672 is enabled when $V_{\overline{EN}}$ is ≤ 0.4V (logic '0'); conversely, the AAT4672 is disabled when $V_{\overline{EN}}$ is ≥ 1.6V (logic '1').

PWRSEL Input

When V_{PWRSEL} is ≤ 0.4V (logic '0') the AUX-OUT current limit is 20% of the current limit value programmed by R_{IAUX}; when V_{PWRSEL} is ≥ 1.6V (logic '1'), the AUX-OUT current limit is 100% of the current limit value programmed by R_{IAUX}.

Current Limit Resistor Selection

The current limits for power supply 1 and power supply 2 inputs are set by resistors between I_{MAIN}/I_{AUX} and GND. The following equation can be used to select the appropriate resistor for a particular current limit:

$$I_{CLMAIN/AUX} = \left(\frac{V_{IMAIN/IAUX}}{R_{IMAIN/IAUX}}\right) \cdot 200k$$

$I_{CLIMAIN/AUX}$	Current limit for MAIN and/or AUX pins respectively
$V_{IMAIN/IAUX}$	Internally Regulated Voltage [0.5V ± 20%] on the IMAIN and IAUX pins respectively
$R_{IMAIN/IAUX}$	IMAIN and/or IAUX Resistor
200k	Internal Gain Factor

Design Example

A particular application requires that the current limit for MAIN be set to 2A and the current limit for AUX be set to 0.2A. What value of resistor is required for the IMAIN and IAUX pins respectively?

For MAIN (power supply 1 input):

$$R_{IMAIN} = \left(\frac{V_{IMAIN}}{I_{CLMAIN}}\right) \cdot 200k$$

$$= \left(\frac{0.5V}{2A}\right) \cdot 200k$$

$$= 50k\Omega \text{ (49.9k}\Omega \text{ standard value)}$$

For AUX (power supply 2 input):

$$R_{IAUX} = \left(\frac{V_{IAUX}}{I_{CLAUX}}\right) \cdot 200k$$

$$= \left(\frac{0.5V}{0.2A}\right) \cdot 200k$$

$$= 500k\Omega \text{ (499.9k}\Omega \text{ standard value)}$$

Thermal Considerations

Since the AAT4672 has an internal current limit and over-temperature protection(thermal shutdown), junction temperature is rarely a concern. However, if the application requires large currents in a high temperature environment, it is possible that temperature rather than current limit will be the dominant regulating condition. In these applications, the maximum current available without risk of an over-temperature condition must be calculated. The maximum internal temperature while current limit is not active can be calculated using Equation 1 (Eq. 1).

Eq. 1: $T_{J(MAX)} = I_{MAX}2 \cdot R_{DS(ON)(MAX)} \cdot R_{\theta JA} + T_{A(MAX)}$

In Equation 1, I_{MAX} is the maximum current required by the load. $R_{DS(ON)(MAX)}$ is the maximum rated $R_{DS(ON)}$ of the AAT4672 at high temperatures (consult the "R_{DSON} vs. Temperature" performance graph in the "Typical Characteristics" section of this datasheet). For estimating the $R_{DS(ON)(MAX)}$ use the data on the "R_{DSON} vs Temperature" performance graph and increase the value from the performance graph by 50%. $R_{\theta JA}$ is the thermal resistance between the AAT4672 die and the printed circuit board (PCB) onto which it is mounted; $R_{\theta JA}$ is the thermal resistance of the TSOPJW-12 package. $T_{A(MAX)}$ is the maximum ambient temperature that the PCB under the AAT4672 would be if the AAT4672 were not dissipating power. Equation 1 can be rearranged to solve for I_{MAX}, into Equation 2 (Eq. 2).

$$\textbf{Eq. 2: } I_{MAX} = \sqrt{\frac{T_{SD(MIN)} - T_{A(MAX)}}{R_{DS(ON)(MAX)} \cdot R_{\Theta JA}}}$$

$T_{SD(MIN)}$ is the minimum temperature required to activate the AAT4672 over-temperature protection (thermal shutdown). With typical specification of 140°C, 125°C is a safe minimum value to use.

For example, for a 2.5V input power supply application that is specified to operate in 50°C environments where the PCB operates at temperatures as high as 85°C. The application is sealed and its PCB is small, causing $R_{\theta JA}$ to be approximately 160°C/W. The $R_{DS(ON)(MAX)}$ is estimated to be 300mΩ (from the "$R_{DS(ON)}$ vs. Temperature" performance graph, where V_{IN} = 2.5V at 85°C plus 50%). To find the maximum current (I_{MAX}) for this application, use Equation 2:

$$I_{MAX} = \sqrt{\frac{125°C - 85°C}{300m\Omega \cdot 160°C/W}} = 0.913A$$

PCB Layout Recommendations

For proper thermal management, to minimize PCB trace resistance, and to take advantage of the low $R_{DS(ON)}$ values of the two internal power switches in the AAT4672, certain circuit board layout rules should be followed: MAIN, AUX, and OUT should be routed using wider than normal traces. The two MAIN pins (1 and 2) and two AUX pins (3 and 4) should be connected to the same wide PCB trace; and GND should be connected to a ground plane. For best performance, input capacitors (C_{MAIN}, C_{AUX}) and output capacitor (C_{OUT}) should be placed as close to the package pins as possible. The AAT4672 evaluation board layout follows the printed circuit board layout recommendations and can be used as an example of an optimal board layout.

Evaluation Board Schematic

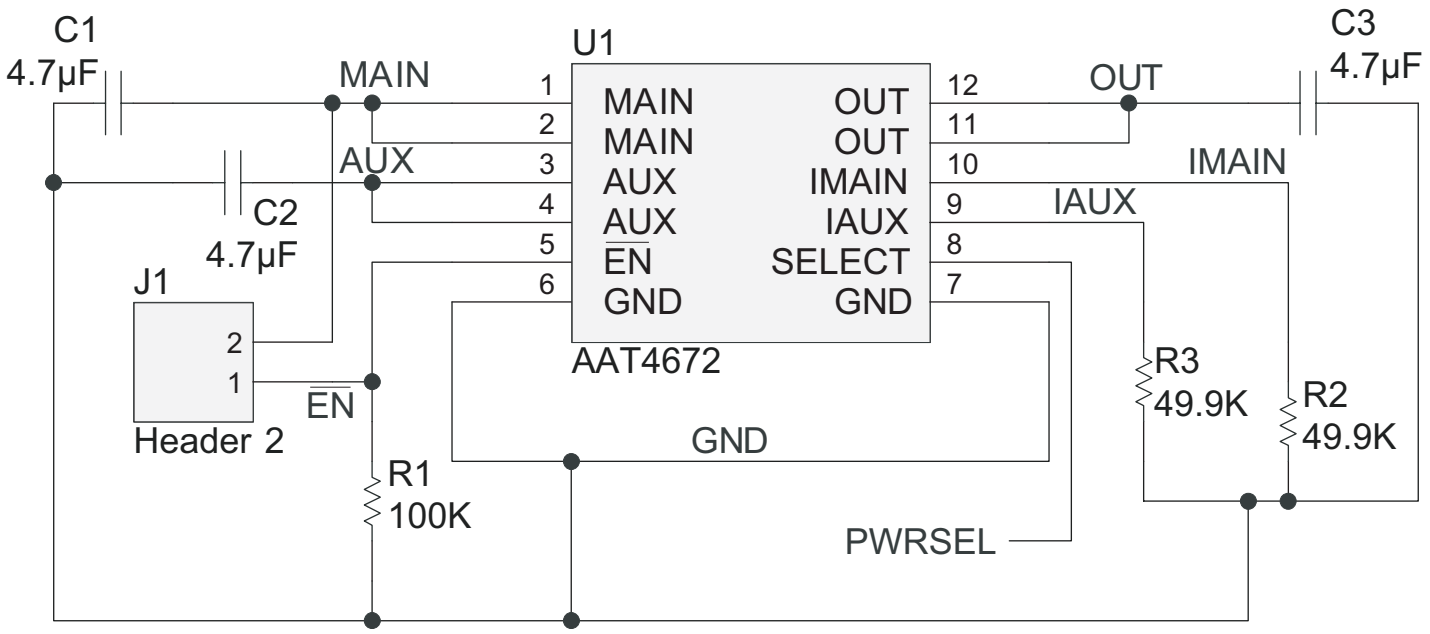


Figure 1: AAT4672 Evaluation Board Schematic.

Evaluation Board Layout

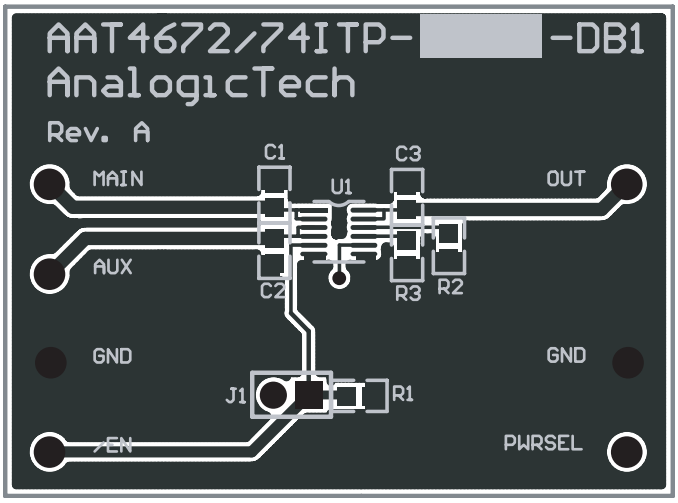


Figure 2: AAT4672 Evaluation Board Top Side Layout.

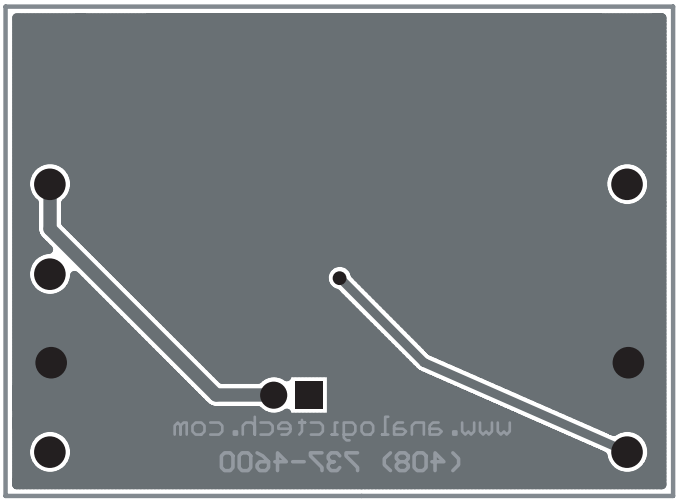


Figure 3: AAT4672 Evaluation Board Bottom Side Layout.

Ordering Information

Package	Marking[1]	Part Number (Tape and Reel)[2]
TSOPJW-12	ZWXYY	**AAT4672ITP-T1**

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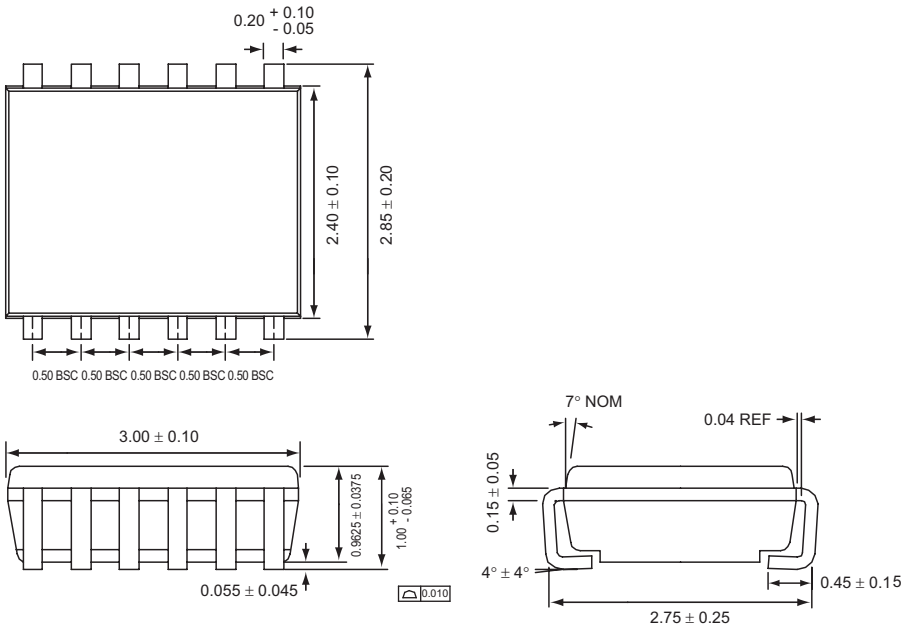
Package Information

TSOPJW-12



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

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